Amendments to the Claims

The listing of claims below will replace all prior versions and listings of claims in the application.

1. (Currently Amended) A latch circuit, comprising:

a bistable pair of transistors connected directly between a reset switch and a first ~~supply voltage~~ node, and having a first port for receiving a first current signal and producing a first output voltage, and a second port for receiving a second current signal and producing a second output voltage; and

a vertical latch having a first transistor and a second transistor and connected directly between said first ~~supply voltage~~ node and a second ~~supply voltage~~ node, said first transistor connected to said first port so that, when said first transistor is turned on, a current flows ~~from said second supply voltage~~ through said first transistor ~~to~~ and said first port, said first transistor is a first type, said second transistor is a second type, and said first type is different from said second ~~type;~~ type.

~~wherein said bistable pair of transistors is connected directly to said first supply voltage.~~

2. (Previously Presented) The latch circuit of claim 1, wherein said first transistor is a MOSFET.

3. (Original) The latch circuit of claim 1, wherein said reset switch is a microelectromechanical reset switch.

4. (Previously Presented) The latch circuit of claim 1, wherein said vertical latch is for decreasing the time necessary for said first port to reach a steady state voltage in response to said first current signal received.

5. (Original) The latch circuit of claim 1, further comprising a vertical latch reset switch connected to said vertical latch.

6. (Currently Amended) The latch circuit of claim 1, further comprising a second vertical latch connected between said first ~~supply voltage~~ node and said second ~~supply voltage~~ node, and connected to said second port.

7-21. (Canceled)